

MIMIC-Compatible GaAs and InP Field Effect Controlled Transferred Electron (FECTED) Oscillators

HELMUT SCHEIBER, KURT LÜBKE, D. GRÜTZMACHER, CHRISTIAN G. DISKUS,
AND HARTWIG W. THIM, SENIOR MEMBER, IEEE

Abstract—An MIMIC-compatible transferred electron oscillator is investigated which utilizes the frequency-independent negative resistance of the stationary charge dipole domain that forms in the channel of a MESFET. Devices fabricated from GaAs and InP exhibit 56 mW at 29 GHz and 55 mW at 34 GHz, respectively. CW power levels are somewhat lower (30 mW). These power levels are the highest ever obtained with lateral transferred electron oscillators and FET oscillators.

I. INTRODUCTION

CONTINUOUS progress during the last few years in the development of millimeter-wave circuits for communication and radar systems has stimulated the search for a planar IC-compatible millimeter-wave source for both local oscillator and VCO applications. The two successfully applied approaches are the GaAs FET oscillator and the planar transferred electron oscillator (TEO).

The intense developments of millimeter-wave FET's has resulted in high-performance oscillators capable of producing 30 mW at 34 GHz with 30 percent efficiency [1] and in a 115 GHz monolithic GaAs FET oscillator [2], which, however, produced a drastically reduced output power of only 0.1 mW. This steep decrease of power cannot be explained merely by the $1/f^2$ law due to the transit time limitation that FET's are subject to. Other effects, such as short-channel effects [3], current injection into the buffer layer, or parasitic bipolar effects [4], must be considered in addition to the difficulty of circuit matching in a three-terminal device. TEO's exhibit lower efficiencies but require simpler loading circuits since they are two-terminal devices. They are much easier to manufacture because submicrometer dimensions are not needed. In addition TEO's are known for their superior noise performance. However, since conventional TEO's are usually operated in

the traveling domain mode ("Gunn oscillations") [5] they also suffer from the transit time ($1/f^2$) limitation, leading to a 6 dB per octave decrease of output power.

A method for circumventing the transit time limitation is to use a planar TEO with an injection limiting cathode contact of the type first described in 1982 [6]. In this device the electron injection is controlled by a negatively biased Schottky gate to the extent that traveling domains cannot form. Instead, a stationary high-field domain forms in the gate-drain region which exhibits a frequency-independent negative resistance. The injection current of the device can be continuously adjusted by the Schottky gate bias voltage, allowing some additional tuning. Computer simulations described in this paper explain the principal operation of the device and show the dependence of power and efficiency on doping level, device length, and operating frequency. Maximum efficiencies obtainable with GaAs devices are of the order of 9 percent at frequencies between 30 and 50 GHz. Experimental efficiencies measured between 30 and 37 GHz are somewhat lower (5 percent) but confirm the absence of the transit time limitation at Ka-band frequencies.

II. DEVICE STRUCTURE

A cross-sectional view of a typical device is shown in Fig. 1. It is similar to a normal MESFET having an extended gate-drain region and an integrated gate-source capacitance. MOCVD-grown n-type GaAs and InP layers have been used. The InP n layer is covered with a thin (100 Å) undoped layer in order to obtain a good Schottky barrier. The active layer doping concentrations have been chosen between $2 \cdot 10^{16} \text{ cm}^{-3}$ and $6 \cdot 10^{16} \text{ cm}^{-3}$ for GaAs and $3 \cdot 10^{16} \text{ cm}^{-3}$ for InP. All devices consist of an ohmic source contact (Ni-Au-Ge), a Schottky anode contact (Ti-Au), and an overlapping Schottky gate contact separated from the source by a 5000-Å-thick chemical vapor deposited SiO_2 layer. The device width is 400 μm . Both the length of the Schottky gate and the distance between gate and source have been chosen to be 0.5 μm . The length of the active region (between gate and anode contact) was varied from 2.3 to 5 μm . The thickness of the semi-insulating substrate is 100 μm .

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H. Scheiber was with the Institut für Mikroelektronik, Universität Linz, A-4040 Linz, Austria. He is now with EBG, Krauss-Str. 1, A-4020 Linz, Austria.

K. Lübke, C. Diskus, and H. W. Thim are with the Institut für Mikroelektronik, Universität Linz, A-4040 Linz, Austria.

D. Grützacher is with the Institut für Halbleitertechnik, Technische Hochschule Aachen, D-5100 Aachen, West Germany.

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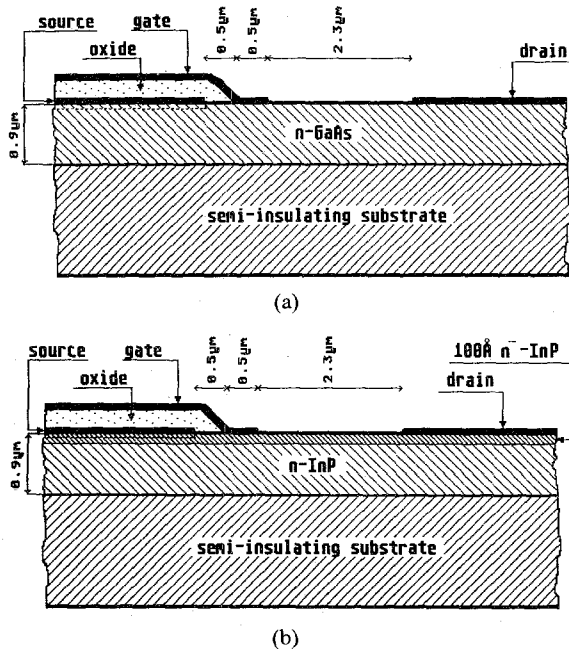


Fig. 1. Cross-sectional view of (a) GaAs and (b) InP devices.

III. DEVICE ANALYSIS AND SIMULATION

It is well known that in a normal MESFET a stationary high-field domain forms in the gate-drain region. The formation of traveling Gunn domains is prevented when the electron injection through the gate is reduced to about 50 percent of the peak current level [7]. Under this condition, a negative differential resistance occurs in the gate-drain region due to the transferred electron ("Gunn") effect.

For better understanding of the whole process, a one-dimensional computer simulation has been performed by solving Poisson's equation, the continuity equation, and the integral current relation. The electron velocity $v(E)$ is calculated using the analytical expression [8].

$$v(E) = \frac{\mu E + v_s (E/E_0)^4}{1 + (E/E_0)^4} \quad (1)$$

According to this equation the velocity is an instantaneous function of local field, thus neglecting delays caused by intervalley scattering and energy relaxation. Hence the results of this analysis are valid only for frequencies up to approximately 60 GHz and for device lengths greater than 1 μm . The structure used in the simulation is shown in Fig. 2. The injection limiting cathode contact represents the one-dimensional equivalent of the gate-source region of a real device. The current I_C injected into the first (left) cell of the device was kept constant in order to properly simulate the saturation current of a MESFET. One-dimensional doping fluctuations as well as a higher doping region at the cathode contact have also been incorporated, as they are known to act as nucleation centers for dipole

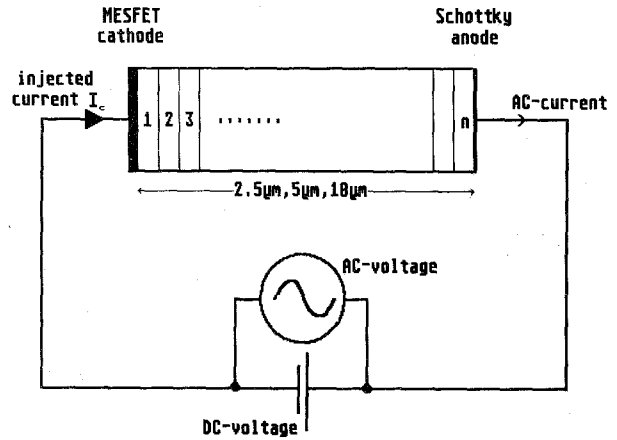


Fig. 2. Simulated device structure and circuit.

TABLE I

average doping level	$1.10^{15} - 5.10^{16} \text{ cm}^{-3}$
device length	2.5 μm ; 5 μm ; 10 μm
DC-voltage	4.5 V - 20 V
amplitude of AC-voltage	4.0 V - 18 V
frequency	25 GHz - 60 GHz

domains in devices with an overcritical $N_D \cdot L$ product. The simulation parameters are summarized in Table 1.

Fig. 3 shows a sequence of field and carrier distributions of a 5- μm -long device calculated at different instants of time and the accompanying voltage and current waveforms. The frequency of operation is 35 GHz, and the dc voltage is 4.5 V; the amplitude of the ac voltage is 3.5 V, allowing a voltage swing down to threshold. As can be seen from Fig. 3 the field is below threshold in a substantial part of the device. This region thus acts as a positive resistance, thereby contributing to loss. It also causes an upper frequency limit (RC limitation). In order to minimize the influence of this lossy region the device length must be kept short.

Fig. 3 also shows that bunches of electrons traverse the depletion region, thereby introducing transit time effects. These effects can enhance efficiency if both the doping level and the bias voltage are chosen properly. Fig. 4 shows calculated efficiencies versus frequency for different doping levels and bias voltages. Higher efficiencies occur at higher frequencies at higher doping levels and lower bias voltages, which can be attributed to adjusting the transit time of the electron bunch close to the oscillation period.

The best calculated efficiencies in the 30–60 GHz range are about 9 percent for GaAs devices and are somewhat higher for InP devices when allowing a current injection of about 58 percent of the peak current. For slightly increased injection current levels the device breaks into traveling domain (Gunn) oscillations at the gate-drain transit time frequency.

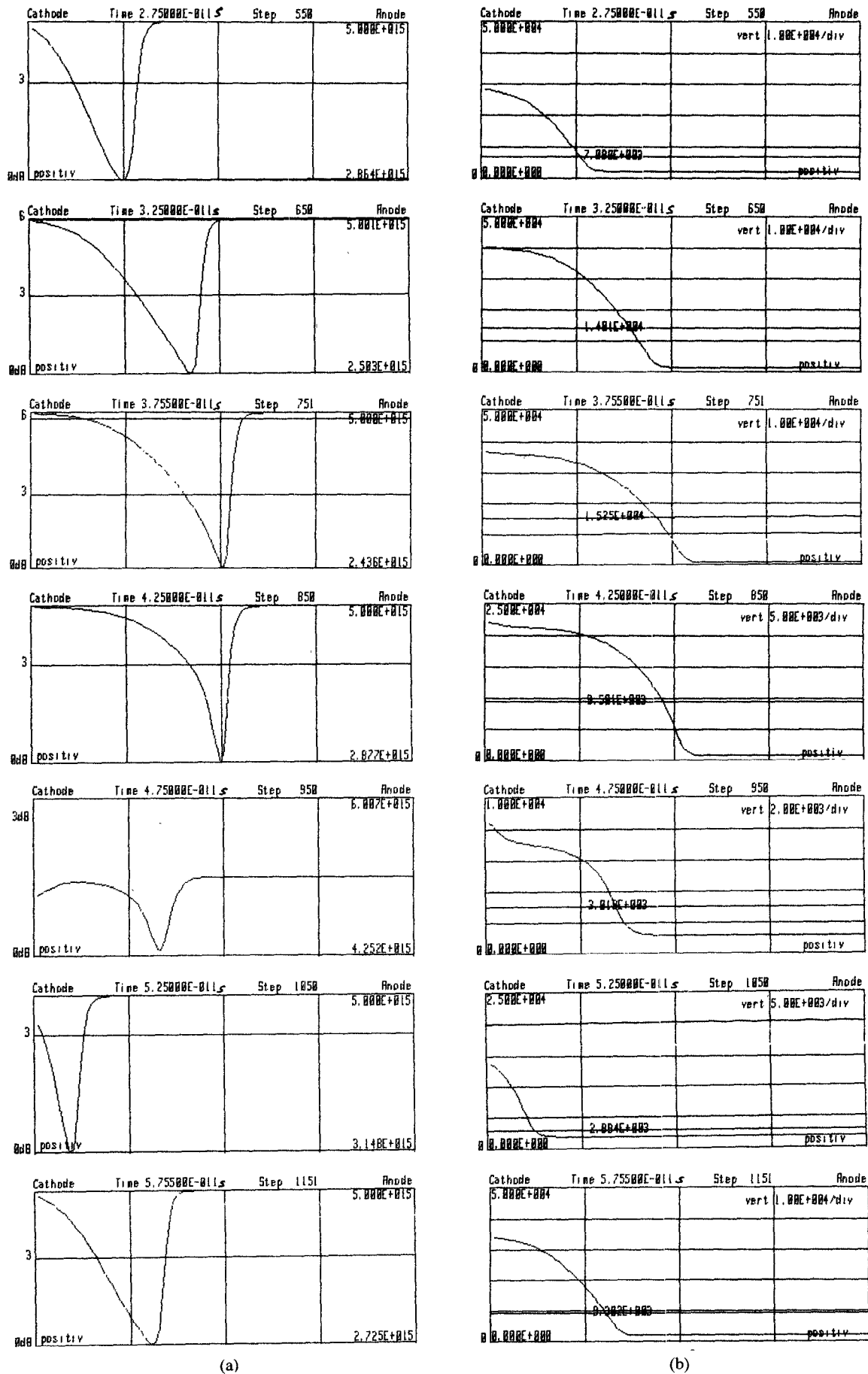


Fig. 3. (a) Calculated carrier concentration. (b) Field distribution. (Continued)

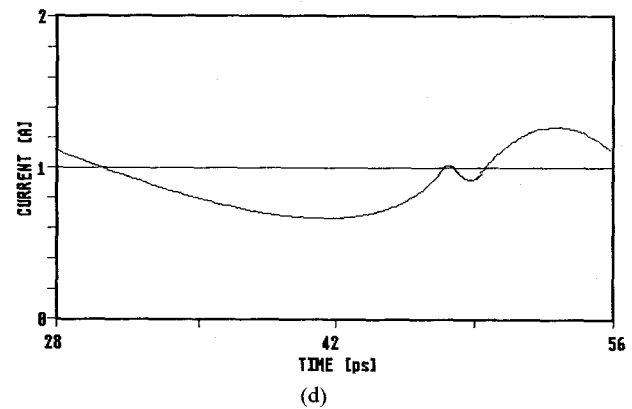
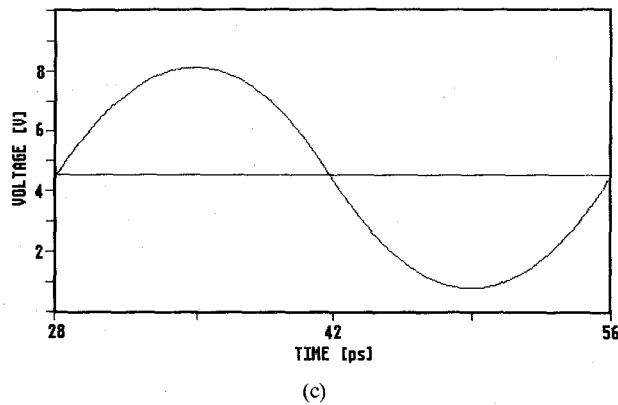


Fig. 3. (Continued) (c) Voltage. (d) Current.

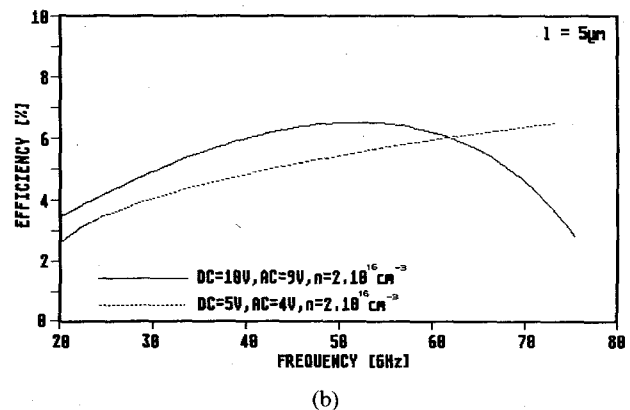
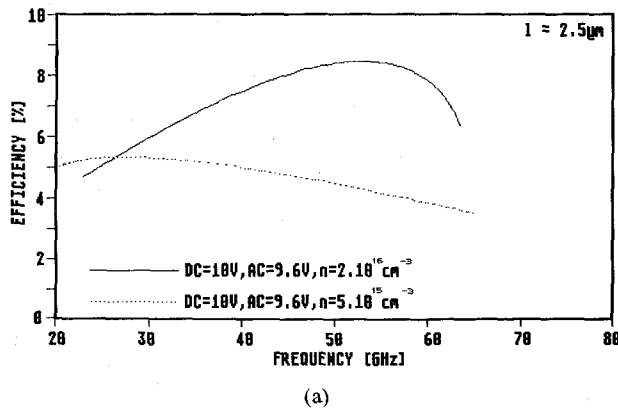
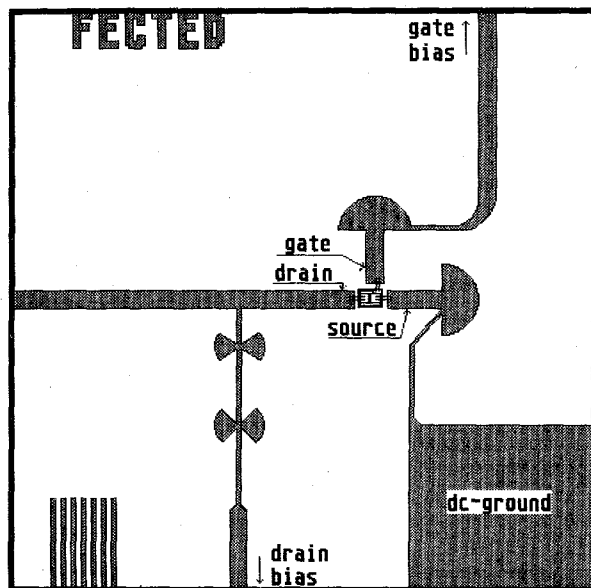
Fig. 4. Calculated efficiencies versus frequency for different voltage and doping levels. (a) $l = 2.5 \mu\text{m}$; (b) $l = 5 \mu\text{m}$.

Fig. 5. Microstrip layout.

IV. EXPERIMENTAL RESULTS

Both GaAs and InP devices have been tested in microstrip circuits fabricated on 250- μm -thick Duroid substrate, as shown in Fig. 5. The device is glued onto the copper heat sink within a rectangular hole cut into the

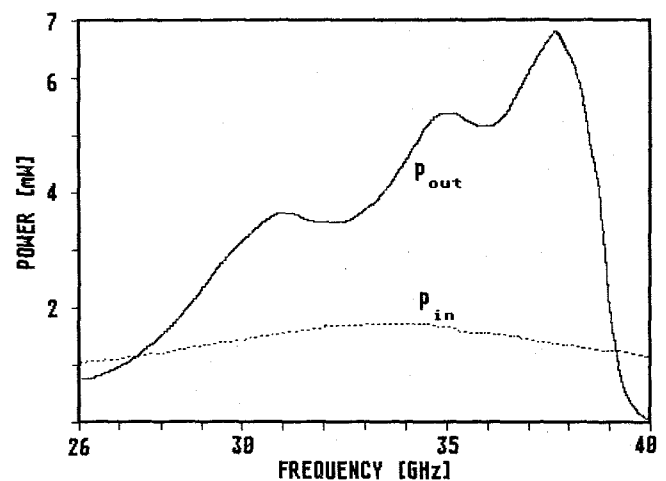


Fig. 6. Input and output powers versus frequency of a FECTED reflection-type amplifier.

Duroid substrate. All three contacts—source, gate, and drain—have been connected to the microstrip circuit using gold bonding wires. The two identical stub-terminated $3\lambda/8$ long transmission lines provide capacitive impedances to both source and gate, compensating bonding wire inductances. With this circuit amplification over almost 10 GHz has been measured with a maximum gain at 37 GHz. A drain voltage of 7.5 V and a negative gate

TABLE II

Material	Drain Bias Pulse Width	V_{DS} (V)	V_{GS} (V)	I (A)	eff. %	P (mW)	f (GHz)
GaAs	1 μ s	7.0	-5.0	0.15	5.3	56	28.4
GaAs	1 μ s	6.1	-7.9	0.13	4.9	39	37.4
InP	1 μ s	11.3	-4.3	0.17	2.9	55	34.4
GaAs	60 μ s	6.7	-8.35	0.15	2.9	29.5	29.8
GaAs	60 μ s	5.4	-9.1	0.144	3.8	29.8	37.3

voltage of -6 V have been applied to this device. Fig. 6 shows measured output power versus frequency with an input power level of approximately 1 mW.

In order to produce free-running oscillations, several resonance circuits have been tested. The best results have been achieved with dielectric resonators placed near the drain contact and by carefully adjusting the gate voltage. Since the frequency of oscillation is determined not only by the dielectric resonator alone but also by the device impedance, the frequency can be shifted by varying the gate bias voltage. Frequency tuning up to 200 MHz at a center frequency of 30 GHz and up to 500 MHz at 37 GHz has been observed.

Table II summarizes the best experimental results. The highest efficiency of a GaAs device at 28.4 GHz for short pulse operation was 5.3 percent. At 37 GHz the efficiency is only a bit smaller, showing the absence of the transit time limitation. A small decrease of efficiency is observed, which is attributed to such parasitic impedances as the drain-gate capacitance.

The efficiencies obtained with InP devices are somewhat smaller owing to the difficulty of making a good Schottky gate contact to InP. Nevertheless, the output power level of InP devices is in the 50 mW range.

In order to prevent burnout, the higher current devices have been tested with long drain pulses. The output power levels obtained with long pulses are generally lower due to the high operating device temperature. This temperature level is believed to be close to that occurring in CW-operated devices since the power output remains unchanged when increasing the duty cycle from 10 to 40 percent.

Fig. 7 shows the spectral characteristics of a free-running 8 mW CW-operated FECTED oscillator. By a crude inspection of this characteristic, one can speculate that FECTED oscillator noise is comparable to conventional Gunn oscillator noise.

V. CONCLUSIONS

It has been shown that GaAs or InP FECTED oscillators are attractive candidates for monolithic millimeter-wave integrated circuits, especially at very high frequencies since they are not transit time limited, as conventional TEO's and FET's are. At 29 GHz and 34 GHz the highest

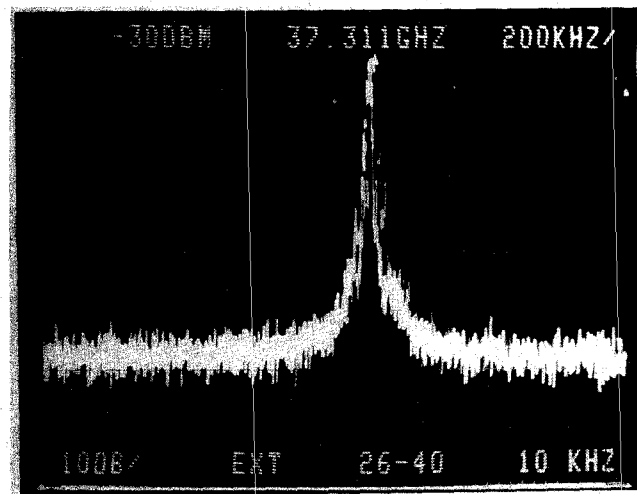


Fig. 7. Spectral characteristic of a free-running 8 mW CW-operated FECTED.

output power levels ever obtained with lateral TEO's and FET oscillators and at 37 GHz the highest lateral TEO output power have been produced. A further increase of output power should be possible by simply increasing the device width as this is not a critical dimension with respect to gate resistance. However, the efficiencies measured at *Ka*-band frequencies are significantly lower than FET oscillator efficiencies but might become comparable at *E*-band and *W*-band frequencies due to the absence of the transit time limitation and to the simpler loading circuitry required by the two-terminal FECTED. However, intervalley scattering and energy relaxation times reduce the effective peak-to-valley ratio at high frequencies, causing an upper frequency limit that FET oscillators are not subject to. This frequency limit has not yet been determined.

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Helmut Scheiber was born in Linz, Austria, on July 3, 1961. He received the Dipl.-Ing. degree in electrical engineering in 1984 from the Technical University of Vienna, Vienna, Austria, and the Ph.D. degree from the University of Linz, Austria.

In 1985 he assumed the position of an Assistant Professor at the Microelectronics Institute of the University of Linz, where he worked on III-V millimeter-wave devices and MIMICS. In July 1989 he joined the Linz-based company EBG, Linz, Austria.

company EBG, Linz, Austria.



Kurt Lübke was born in Salzburg, Austria, on May 18, 1942. He received the Dipl.-Ing. degree in physics in 1973 and the Ph.D. degree in electrical engineering in 1980, both from the Technical University of Vienna, Vienna, Austria.

In 1973 he became an Assistant Professor at the Industrial Electronics Institute, Technical University of Vienna, where he worked on III-V semiconductor device Technology. In 1985 he joined the Microelectronics Institute at the University of Linz, Austria, where he established a

III-V submicrometer-technology laboratory. His area of research is in submicrometer lithography and MOCVD growth of III-V semiconductor devices for high-speed and microwave applications.



D. Grützmacher was born in Hamburg, West Germany, on August 28, 1960. He received the Diplom Physiker degree from the Technical University of Aachen, Aachen, West Germany, in 1988. He is currently working toward the Ph.D. degree in physics at the Technical University of Aachen under Prof. Balk. His research focuses on LP-MOVPE growth of GaInAsP alloys on InP substrates for optoelectronics, in particular the deposition of GaInAs/InP multiple-quantum-well structures for 1.3 μm lasers.



Christian G. Diskus was born in Linz, Austria, on December 19, 1959. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Graz, Austria, in 1984.

In 1985 he became an Assistant Professor at the Microelectronics Institute, University of Linz, where he has been engaged in research and development work on III-V semiconductor devices for high-speed applications.



Hartwig W. Thim (M'65-SM'86) was born in Wels, Austria, in 1935. He received the Diplom-Ingenieur in 1960, and the Doctor of Technical Sciences in 1964, both from the Technical University of Vienna, Vienna, Austria.

In 1960 he became an Assistant Professor at the Technical University of Vienna, where he lectured and worked on dielectric rod antennas. In 1964 he joined Bell Telephone Laboratories, Murray Hill, NJ, where he did research and development work on bulk semiconductor de-

vices, vanadium dioxide films, and millimeter-wave p-i-n diode switches. He developed the first stable bulk semiconductor amplifier, known as the TEA (transferred electron amplifier), together with coworkers at Bell Labs. In 1969 he became head of the microwave device physics group at the Fraunhofer Institute for Applied Solid State Physics, Freiburg, West Germany. In this position he was responsible for the development of new microwave semiconductor and acoustic surface wave devices. In 1974 he became a full Professor in the Electrical Engineering Department of the Technical University of Vienna, and in 1985 he moved to the University of Linz, Linz, Austria, where he heads the Microelectronics Institute. His research interests include crystal growth of compound semiconductor materials, bulk semiconductor and heterojunction devices for microwave and millimeter-wave applications, GaAs integrated circuits, sensors, and microprocessor applications.